IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION No. : 09/993,094 Group Art Unit : 2841
FILING DATE : November 6, 2001 Examiner :VU, PHUONG T
TITLE : Adapter Device, Memory Device and Integrated Circuit Chip

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

SIR:

CERTIFIED TRANSLATION

I, Takashi Narita, am an official translator of the Japanese language into the English language and I hereby certify that the attached comprises an accurate translation into English of Japanese Application No. 2000-344453, filed on November 10, 2000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

September 21, 2005

Date

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[Document Name] Patent Application

[Reference Number] 0000967702

[Filing Date] November 10, 2000

[To] Hon.Commissioner, Patent Office

[IPC] G11C 25/00

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[Indication of Charge]

[Number of Prepaid Ledger] 019530

[Amount] 21,000 yen

[List of Document]

[Document] Specification 1

[Document] Drawing 1

[Document] Summary 1

[General Power of Attorney Number] 9707387

[Need of Proof] Yes

[Name of Document] SPECIFICATION

[Title of the Invention]

Memory Device and Integrated Circuit Chip used for the same

[Claims]

[Claim 1]

A memory device comprising:

a substantially rectangular main body unit loaded on a host apparatus;

one or a plurality of memory chips each including a memory device therein;

a first connection terminal provided to one side of said main body unit for electrical connection to said host apparatus;

loading sections provided in succession to an inserting opening which is formed in the opposite side of said main body unit and through which said memory chip is inserted, said loading section(s) being adapted for loading said memory chip therein, with the number of said loading section(s) corresponding to the number of the memory chips that may be loaded on said main body unit; and

a second connection terminal provided to said loading section(s) and configured for being electrically connected to a set of terminals provided to said memory chip(s);

said main body unit including a controller for controlling write and readout of information signals to or from one or more memory chip(s) loaded in said loading section(s).

[Claim 2]

The memory device according to claim 1 wherein the main body unit has a size of a short side of approximately 21.45 mm, a size of a long side of approximately 50 mm and a size of a thickness of approximately 2.8 mm.

[Claim 3]

The memory device according to claim 1 wherein a further chip of the same shape as said memory chip may be loaded in said loading section(s) of said main body unit, said further chip having enclosed therein a semiconductor integrated circuit device forming a logical circuit.

[Claim 4]

The memory device according to claim 1 wherein said memory device is a flash memory.

[Claim 5]

An integrated circuit chip inserted into and ejected from a substantially rectangular main body unit, loaded in a host apparatus, said integrated circuit chip having enclosed therein an integrated circuit device controlled by a controller enclosed in said main body unit, comprising:

a main chip body unit having said integrated circuit device enclosed therein and adapted for being inserted into and ejected from a loading section provided to said main body unit; and

a set of terminals provided to one side of said main chip body unit and adapted for being connected to connection terminals provided to said loading section to

exchange information signals between said controller and the integrated circuit device.

[Claim 6]

The integrated circuit chip according to claim 5 wherein said integrated circuit device is a flash memory.

[Claim 7]

The integrated circuit chip according to claim 5 wherein said integrated circuit device is a logical circuit chip.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

This invention relates to a memory device that has a main body unit that can be mounted or dismounted to or from a host equipment, to or from which main body unit a memory chip can be mounted or dismounted, and a integrated circuit chip that can be mounted or dismounted to or from the main body unit used in the memory device.

[0002]

[Prior Art]

As external memory device for an information processing apparatus, such as a personal computer or a digital still camera, there is a substantially plate-shaped memory device employing a semiconductor memory as a recording medium. The memory device of a larger storage capacity is able to store information signals up to a higher value of approximately 64 Mbytes.

[0003]

[Problems to be Solved by the Invention]

If this memory device is used as an external storage device, such as a digital still camera, picture data having a larger data size is manipulated. Since these numerous picture data cannot be stored in a sole memory device, the user has to purchase a new memory device.

[0004]

There are occasions where music air data or data processed by a computer are stored on this memory device in addition to the picture data. If many sorts of data are are stored in a sole memory device, it may be an occurrence that the user forgets data stored on the memory device, with the result that data management becomes complex in order to prevent this from occurring.

[0005]

Moreover, in saving digital contents, protected by the copyright, such as music air data, in the memory device, a copyright management function needs to be provided in order to prohibit unauthorized copying of digital contents. Thus, in the memory device, it may become necessary to add a function capable of coping with different sorts of information signals to be saved.

[0006]

It is therefore an object of the present invention to provide a novel memory device in which a memory chip can be mounted on or dismounted from the main body

unit of the device to enable the storage capacity to be varied depending on the objective of using the memory device by the user to improve convenience in use of the memory device.

[0007]

It is another object of the present invention to provide a novel memory device in which a chip with a built-in integrated circuit unit having a function distinct from the memory function can be loaded on a loading portion of the memory chip to enable new functions to be added readily.

[0008]

It is still another object of the present invention to provide an integrated circuit chip having built therein an integrated circuit unit that can be mounted to or dismounted for a main body unit that can be mounted to or dismounted from the host equipment and that is aimed at annexing a variety of functions to an external device of the host device.

[0009]

[Means to Solve the Problem]

According to the present invention, there is provided a memory device including: a substantially rectangular main body unit loaded on a host apparatus; one or a plurality of memory chips each including a memory device therein; a first connection terminal provided to one side of said main body unit for electrical connection to said host apparatus; loading sections provided in succession to an inserting opening which

is formed in the opposite side of said main body unit and through which said memory chip is inserted, said loading section(s) being adapted for loading said memory chip therein, with the number of said loading section(s) corresponding to the number of the memory chips that may be loaded on said main body unit; and a second connection terminal provided to said loading section(s) and configured for being electrically connected to a set of terminals provided to said memory chip(s); said main body unit including a controller for controlling write and readout of information signals to or from one or more memory chip(s) loaded in said loading section(s).

[0010]

According to the present invention, there is also provided a an integrated circuit chip inserted into and ejected from a substantially rectangular main body unit, loaded in a host apparatus, said integrated circuit chip having enclosed therein an integrated circuit device controlled by a controller enclosed in said main body unit, including: a main chip body unit having said integrated circuit device enclosed therein and adapted for being inserted into and ejected from a loading section provided to said main body unit; and a set of terminals provided to one side of said main chip body unit and adapted for being connected to connection terminals provided to said loading section to exchange information signals between said controller and the integrated circuit device.

[0011]

[Preferred Embodiment of the Invention]

Referring to the drawings, a memory device and an integrated circuit chip used as this memory device, according to the present invention, will be explained in detail.

[0012]

Referring to Fig.1, the memory device 10 is used as an external storage device for a host equipment 1, such as personal computer, a digital still camera, a digital video camera or an audio equipment. In this memory device 10, information signals, such as data processed by a computer, picture data, video data or music air data, are stored. The memory device 10 is loaded on the host equipment 1 through an insertion/ejection opening 2 provided in the host equipment 1, as shown in Fig.1, for recording and/or reproducing information signals.

[0013]

The memory device 10, used as described above, is in a substantially rectangular shape, with the length of a short side W1 being approximately 21.45 mm, a length of a long side W2 being approximately 50 mm and with the thickness W3 being 2.8 mm, as shown in Fig.2, Fig.3, Fig.4, and Fig.5.

[0014]

This plate-shaped memory device 10 includes a casing 11, made up of an upper half 10a and a lower half 10b, forming the main body unit of the device. The upper half 10a and the lower half 10b, making up the casing11, is formed by molding a rigid synthetic resin material. Within the casing 11, formed by bonding the upper half 10a and the lower half 10b, there is enclosed a semiconductor unit 12 operating as a

controller for managing the writing and the readout of information signals. The casing 11 is formed to exhibit mechanical strength such that the casing 11 is not bent with a usual external force that may be applied during use to protect the internal semiconductor unit 12.

[0015]

On one short side of the casing 11 is formed a terminal unit 13 for extending from a front surface 11a to a bottom surface 11b. In this terminal unit 13, a number of engagement recesses 15 corresponding to the number of electrodes are formed by being delimited by partitioning walls 14. These engagement recesses 15 are engaged by terminals provided on the host equipment 1. A plural number of the electrodes 16, separated from one another by the partitioning walls 14, are provided on the bottom surfaces of these engagement recesses 15. The electrodes 16, thus provided on the bottom surfaces of the engagement recesses 15, may be protected by the engagement recesses 15 from being directly touched by the user's hand or finger. The present casing 11 is provided with ten electrodes 16. Data exchange with the host equipment 1 is via the electrodes 16 provided in the terminal unit 13 over a serial interface. Specifically, the plural electrodes 16 are at least input terminals for serial protocol bus state signals BS, an input terminal for serial protocol data SDIO and an input terminal of serial clocks SCLK, in addition to a power source voltage VCC terminal and a reserve terminal.

[0016]

On one corner towards the front side 11a carrying the terminal unit 13 of the casing 11 is formed a cut-away portion 17 for allowing the user to discern the direction of insertion of the casing into the host equipment 1. In a lateral surface of the casing 11 in which is formed the cut-away portion 17, there is formed a mistaken insertion prohibiting groove 18 opened in the bottom surface 11b in continuation to the cut-away portion 17. When loading the memory device 10 on the host equipment 1, the cut-away portion 17 and the mistaken insertion prohibiting groove 18 control the direction of insertion of the memory device 10 into the host equipment 1 to prevent mistaken insertion. That is, if the memory device 10 has not been introduced in a regular condition via insertion/ejection opening 2, the cut-away portion 17 and the mistaken insertion prohibiting groove 18 prohibit the electrodes 16 and the set of terminals provided on the host equipment 1 from contacting the engagement recesses 15 delimited by the partitioning walls 14 to prevent the electrodes 16 from contacting the set of terminals provided on the host equipment 1.

[0017]

In one lateral surface 11c of the casing 11 towards its one front surface 11a is formed a detachment preventative recess 19 opened in the bottom surface 11b. When the casing 11 is inserted into the host equipment 1, the detachment preventative recess 19 is engaged with a resilient engagement piece provided on the host equipment 1 to prevent the detachment of the casing 11 from the host equipment 1. At a mid portion towards the other lateral surface 11d of the casing 11 is formed an engagement recess

21 opened in the bottom surface 11b. The engagement recess 21 is adapted for engaging with an ejection mechanism provided on the host equipment 1.

[0018]

Referring to Figs.2 and 6, three loading sections 22 are provided side-by-side along the length of the casing 11 for loading or unloading memory chips 27. These loading sections 22 are provided in continuation to insertion/ejection openings 23 formed in one lateral surface 11c of the casing 11. In a planar surface 11e of the casing 11 formed by the upper half 10a is formed an opening 24 through which the memory chips 27 can be inserted or ejected with the user's hand or finger. These loading sections 22 are formed to the same size as the memory chips 27, such that, when the memory chip 27 is loaded in position, the back surface 28e facing outwards via insertion/ejection opening 23 of the memory chip 27 will be flush with the lateral surface 11c of the casing 11. By so doing, the back surface of the memory chip 27 is not protruded from the lateral surface 11c when the memory chip 27 is mounted on the loading section 22, with the result that insertion or ejection of the host equipment 1 may be performed smoothly with optimum hand feeling.

[0019]

The bottom surface 22a of the loading section 22 also operates as insertion or ejection guide in inserting or ejecting the memory chip 27. In the innermost part of the loading section 22, there are provided connection terminals 25 for establishing electrical connection with respect to the memory chip 27. In the lateral surface 22b

in the loading section 22, parallel to the inserting direction of the memory chip 27, and in the lateral surface 22c thereof against which abuts the inserting end of the memory chip 27, there is formed a guide recess 26 for guiding the insertion or ejection of the memory chip 27 and for controlling its loading position.

[0020]

The memory chip 27, mounted on the loading section 22, includes a substantially rectangular main body unit of the chip 28 of substantially the same size as the loading section 22, molded of the same material as the casing 11, as shown in Fig.6. Within the main body unit of the chip 28 is enclosed one flash memory 29 as a semiconductor memory. The flash memory 29 has a storage capacity of, for example, 4 MB, 8 MB, 32 MB, 64 MB, 128 MB, ···.

[0021]

On the bottom surface 28b towards the inserting end to the loading section 22 of the main body unit of the chip 28, that is towards its front side 28a, there are provided a plural number of terminals 31 electrically connected to the connection terminals 25 provided on the loading section 22. By these terminals 31 being electrically connected to the connection terminals 25 of the loading section 22, data can be written on or read out from the flash memory 29 by a control circuit provided on the casing 11.

[0022]

On a portion of the bottom surface 28b towards the front surface 28a of the

main body unit of the chip 28 and towards both lateral surfaces 28c, 28d neighboring to the front surface 28a is protuberantly formed a guide section 32 adapted for guiding the insertion of the main body unit of the chip 28 into the loading section 22. This guide section 32 is engaged in the guide recess 26 formed in the loading section 22 to guide the insertion or ejection of the memory chip 27.

[0023]

In order to prevent detachment of the memory chip 27, mounted on the loading section 22, a detachment preventative member may be provided in the vicinity of the insertion/ejection openings 23. The number of the loading sections 22 may be one, two or not less than four instead of three.

[0024]

The circuit structure of the memory device 10 and the host equipment 1 on which the memory device 10 is mounted is now explained with reference to Fig.7.

[0025]

First, the circuit structure of the memory device 10 is explained. A controller 41, provided in the semiconductor unit 12 in the casing 11 of the memory device 10 includes a memory controller 42 for controlling data writing or readout to or from the flash memory 29 of the memory chip 27, a register 43 having a variety of parameters for data writing or readout, a page buffer 44 for transient data storage and a serial/parallel/serial interface (S/P·P/S interface) 45 for data exchange with the host equipment 1. The casing 11, forming the main body unit of the memory device 10,

includes a chip interface 46 for data exchange between the flash memory 29 of the memory chip 27 and the controller 41 of the casing 11. The chip interface 46 enables data exchange between the controller 41 and a chip having a variety of functions when the chip is mounted on the loading section 22.

[0026]

The memory chip 27, mounted on or dismounted from the casing 11, includes a sole flash memory 29 and a chip interface 47 connected to the chip interface 46 to effect data exchange with the controller 41.

[0027]

By way of explaining the circuit structure of the host equipment 1, the host equipment 1 includes a file manager 51 performing file management of the memory device 10, a transfer protocol interface 52 for executing access to a register 43 or to a page buffer 44 of the controller 41 of the memory device 10, and a serial interface 53 providing for the protocol necessary for data transfer over three signal lines, namely the serial clock SCLK, bus state BS and the serial data input/output SDIO. The file manager 51 is realized by a controller, such as CPU, of the host equipment 1executing the application.

[0028]

By way of explaining the method of using the memory device 10, the memory chip 27 is inserted into the casing 11 via the insertion/ejection openings 23 provided in the lateral surface 11c of the casing 11, with the front surface 28a carrying the

terminal 31 as the inserting end, as shown in Fig.6. At this time, the memory chip 27 is inserted into the loading section 22 via insertion/ejection openings 23 as the guide section 32 is engaged with the guide recess 26 formed in the loading section 22. Thus, the user is able to insert the memory chip 27 smoothly into the loading section 22. When the insertion of the memory chip 27 comes to a close, the chip interface 47 on the side memory chip 27 shown in Fig.7 is connected to the chip interface 46 on the casing 11.

[0029]

When the loading of the memory chip 27 on the loading section 22 comes to a close, the back surface 28e of the main body unit of the chip 28 forming the memory chip 27 is substantially flush with the lateral surface 11c of the casing 11 provided with the insertion/ejection openings 23. Thus, the memory device 10 is able to insert the memory chip 27 smoothly into the host equipment 1. Moreover, the user may be safeguarded from having an objectionable touch feeling when holding the memory device 10 with his or her hand.

[0030]

It is unnecessary to have memory chips 27 mounted in all of the loading sections 22 provided in the casing 11, but only one or two memory chips 27 may suffice. Moreover, not only the memory chips 27 of the same storage capacity but also those having different storage capacities may be loaded. Therefore, the user is able to set the overall storage capacity of the memory device 10 depending on the use

objects. Moreover, the user is able to load such memory chips 27 classified depending on data sorts to the respective loading sections 22 such as by loading a memory chip 27 having musical numbers stored therein, a memory chip 27 having picture data stored therein, and a memory chip 27 having data for processing by a computer stored therein. This enables the user to perform data management extremely readily.

[0031]

The memory chip 27 can be taken from the casing 11 extremely readily by sliding the memory chip 27, facing outwards via opening 24, towards the insertion/ejection openings 23.

[0032]

The memory device 10, in at least one of the loading sections 22 of which the memory chip 27 is loaded, is inserted via insertion/ejection opening 2 of the host equipment 1, with the front surface 11a carrying the terminal unit 13 of the casing 11 as an inserting end, as shown in Fig.1. It is noted that the cut-away portion 17 and the mistaken insertion prohibiting groove 18 are provided in the front surface 11a of the casing 11. Thus, if the memory device 10 is inserted via insertion/ejection opening 2 of the host equipment 1 under a non-usual condition, for example, in the upside-down condition, the memory device 10 cannot be inserted, thus prohibiting the mistaken insertion. If the memory device 10 is inserted into the loading section of the host equipment 1, the detachment preventative recess 19 formed in the memory

device 10 is engaged by e.g., an elastic engagement portion provided on the loading section of the host equipment 1 to provide for positive mounting on the loading section to prevent inadvertent detachment.

[0033]

When the memory device 10 is loaded on the host equipment 1, the electrode 16 is caused to contact the set of terminals provided on the host equipment 1 so that the S/P·P/S interface 45 on the side memory device 10 is connected to a serial interface 53 on the host equipment 1, as shown in Fig.7. The S/P·P/S interface 45 then is fed from the host equipment 1 with the serial protocol bus state signals BS and serial clocks SCLK. The controller supervising the entire host equipment 1 executes the application to realize the file manager 51 which then reads out the data information, such as filename or data size, from the flash memory 29 of the memory chip 27 loaded in the loading section 22 of the casing 11.

[0034]

When writing data in the flash memory 29 of the memory chip 27, the file manager 51 updates itself, at the same time as it outputs data to the memory device 10 through a transfer protocol interface 52 and a serial interface 53. Based on a control signals from the file manager 51, the memory controller 42 causes data input from the host equipment 1 to be transiently stored in a page buffer 44 through S/P·P/S interface 45 in accordance with the serial protocol bus state signals BS and the serial clocks SCLK. The memory controller 42 then causes data to be stored through the chip

interfaces 46, 47 in the flash memory 29 of the preset memory chip 27.

[0035]

When reading out data stored in the flash memory 29 of the preset memory chip 27, the memory controller 42 reads out data to the page buffer 44 from the flash memory 29 of the preset memory chip 27, in accordance with the serial protocol bus state signals BS and the serial clocks SCLK, to output the read-out data to the host equipment 1 through the S/P·P/S interface 45. The file manager 51 reads out data through the serial interface 53 and the transfer protocol interface 52.

[0036]

Meanwhile, the memory device 10, loaded on the loading section 22 of the host equipment 1, is ejected to outside via insertion/ejection opening 2 by an ejection mechanism engaged in the engagement recess 21 formed in the casing 11.

[0037]

Meanwhile, the memory chip 27 may be used by itself as an external storage device for the host equipment 1. At this time, the casing 11 forming the main body unit of the memory device 10 operates as an adapter device in reading out or writing data by a host equipment 1 that does not use the memory chip 27 as an external storage device.

[0038]

With the above-described memory device 10, the overall storage capacity may be set solely by exchanging the memory chip 27. The user is able to change the

entire storage capacity depending on the use object to improve convenience in use. The user is also able to put the memory device 10 to different uses from one loading section 22 to another. That is, the memory chip 27 mounted on the first loading section 22 may be used to store music airs, while the memory chip 27 mounted on the second loading section 22 may be used to store picture data and the memory chip 27 mounted on the third loading section 22 may be used to store processing data to be processed by a computer. So, the user may feel easy in supervising the data. Moreover, if a further memory is required, it is only sufficient if the user purchases only the memory chip 27 so that the user may be relieved of excess expenses.

[0039]

Meanwhile, an integrated circuit unit having a built-in logic circuit may be enclosed as an integrated circuit unit in the main body unit of the chip 28 in addition to the aforementioned flash memory 29.

[0040]

For example, in the embodiment shown in Fig.8, the memory chip 27 is mounted in each of the address 1 loading section 22 and address 2 loading section 22, whilst a copyright protection chip 61 is mounted on the address 3 loading section 22. If the memory chip 27 is mounted in each of the address 1 loading section 22 and address 2 loading section 22 and digital contents such as music air data or picture data of digital signals protected for copyrights are saved in these memory chips 27, it is necessary to protect e.g., the ID of the user in order to prevent illicit copying of the

digital contents saved in these memory chips 27. Thus, in the present memory device, the user ID, for example, is stored in an address 3 in the main body unit of the chip 28 in the present memory device, whilst the copyright protection chip 61 having a built-in integrated circuit chip having a logic circuit capable of authentication mounted therein is mounted in the address 3 loading section 22. This gives a memory device having the function of protecting the copyrights.

[0041]

In the embodiment shown in Fig.9, the memory chip 27 is loaded on the address 1 loading section 22, the transmission/reception circuit chip 62 is mounted on the address 2 loading section 22 and an antenna chip 63 is loaded on the address 3 loading section 22. This guarantees data transmission/reception between different memory devices.

[0042]

Of course, there is no particular limitation to the addresses of the loading sections 22 mounting these chips 27, 61, 62 or 63.

[0043]

With the memory device according to the present invention, as described above, since integrated circuit chips having a variety of functions may be loaded on the loading section 22 of the casing 11, a variety of functions may be annexed to the memory function with the use of the sole casing 11.

[0044]

[Effect of the Invention]

With the memory device of the present invention, since the overall storage capacity can be set solely by exchanging the memory chips, the user is able to change the storage capacity of the memory device depending on the use object to improve the convenience in use of the memory device. Moreover, the user is free to select the memory chip application from one loading section to another, with the result that the user is able to manage the data readily. In addition, if a further memory is required, the ser only has to purchase a memory chip, and hence may be relieved of redundant economic loads.

[0045]

With the integrated circuit chip according to the present invention, by employing a memory device, a copyright protective circuit unit, a transmission/reception circuit unit, an antenna unit or a power source unit as the integrated circuit unit enclosed in the main body unit of the chip, a variety of functions may be annexed to the memory device to enlarge the application of the memory device.

[Brief Description of the Drawings]

Fig.1 illustrates the mode of using a memory device embodying the present invention.

Fig.2 is a plan view showing the memory device.

Fig.3 is a front view thereof.

Fig.4 is a bottom view thereof.

Fig.5 is a side view thereof.

Fig.6 is a perspective view for illustrating a memory chip that can be mounted on or dismounted from the memory device and a loading unit for loading the memory chip.

Fig.7 is a block diagram for illustrating a circuit structure of the memory device and the host equipment.

Fig.8 illustrates an instance of loading a memory chip and a copyright protection chip on a loading unit provided on a casing.

Fig.9 illustrates an instance of loading a memory chip, a transmission/reception circuit chip and an antenna chip.

[Explanation of Referenced Numerals]

1 Host equipment

2 Insertion/ejection opening

10 Memory device

11 Casing

12 Semiconductor unit

13 Terminal unit

22 Loading sections

23 Insertion/ejection openings

24 Opening

25 Connection terminals

26 Guide recess

27 Memory chip

28 Chip

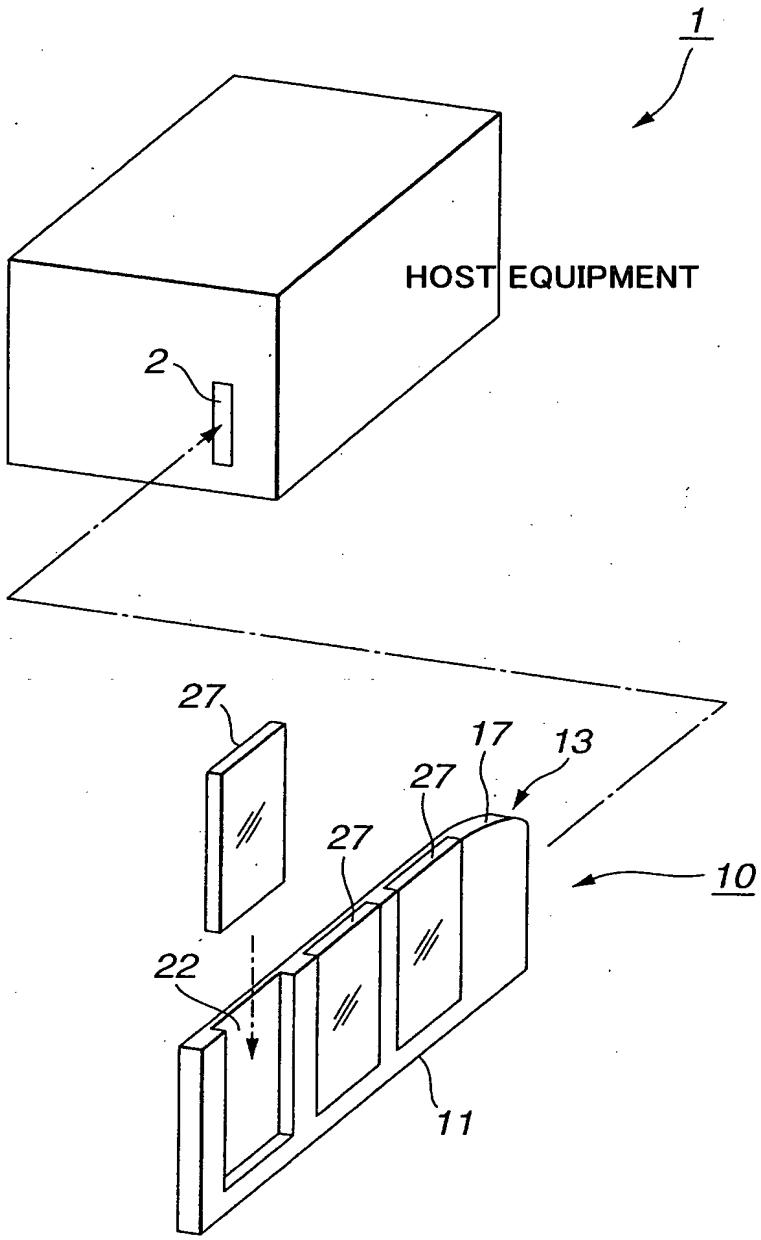
29 Flash memories

31 Terminals

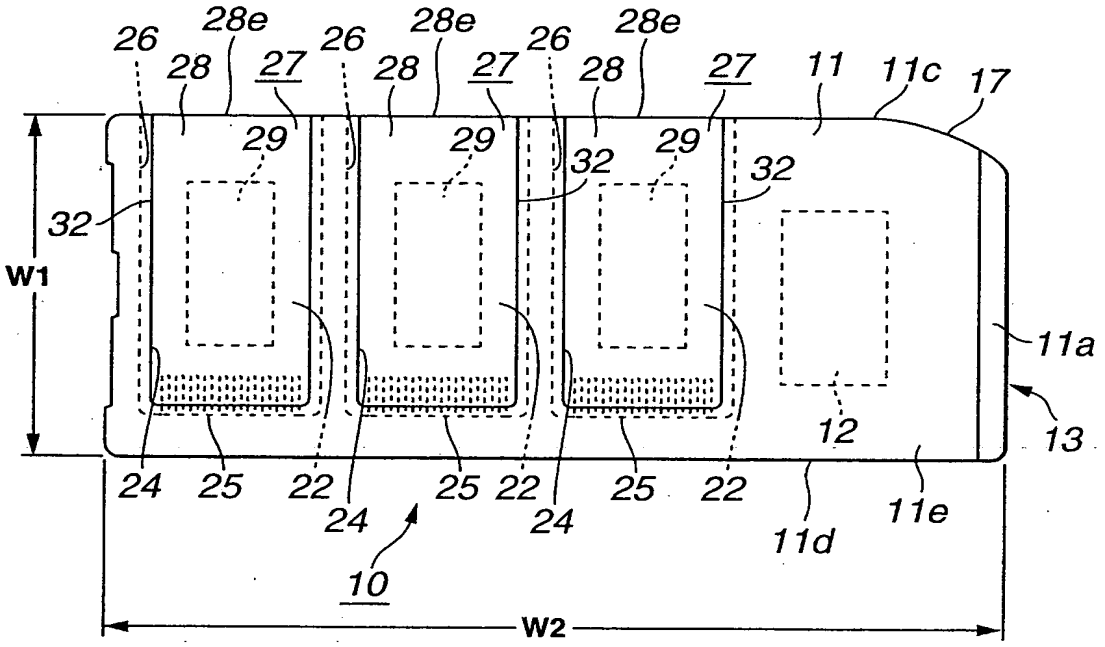
32 Guide section

[DOCUMENT NAME] DRAWING

[FIG.1]



[FIG.2]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W1
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11d
11e
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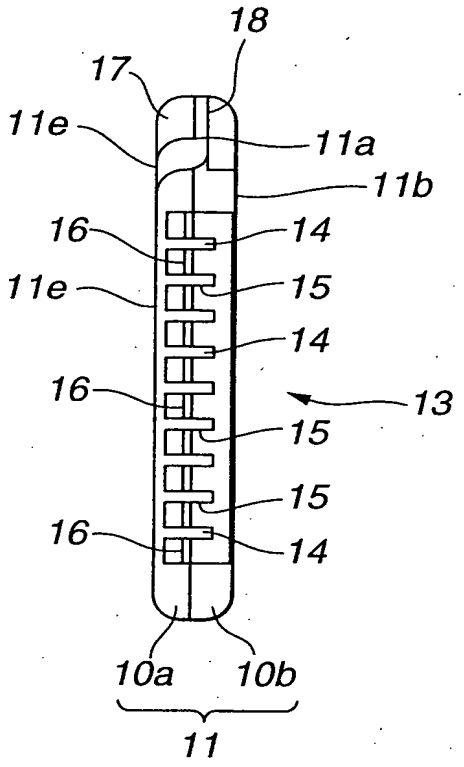
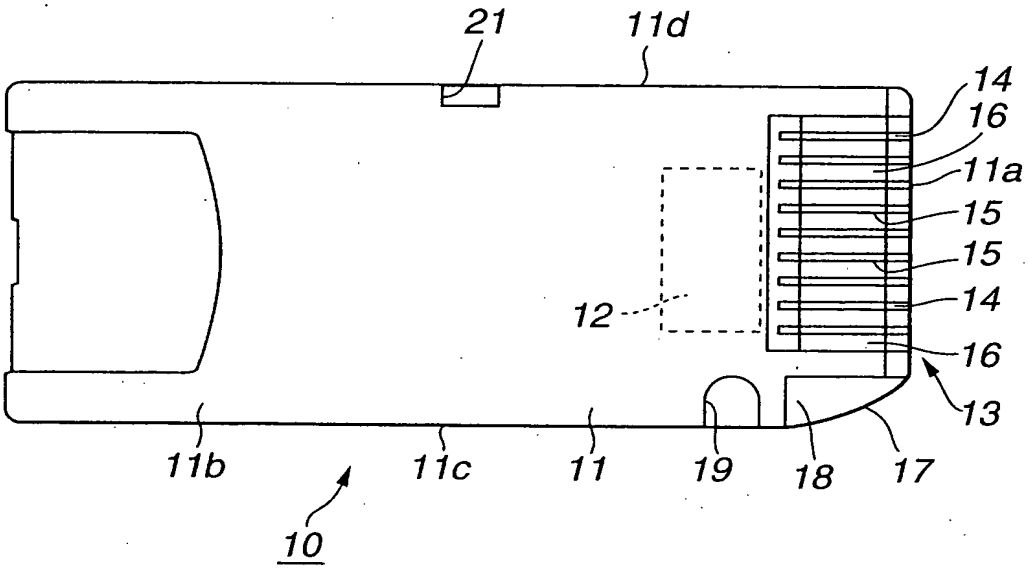
W2

[FIG.3]



[FIG.4]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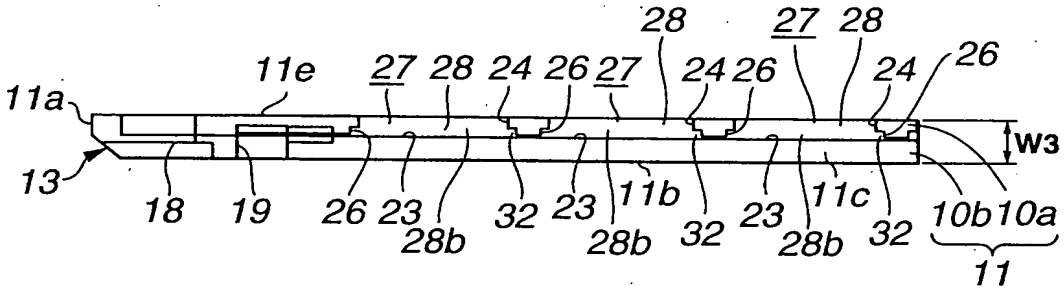
[FIG.5]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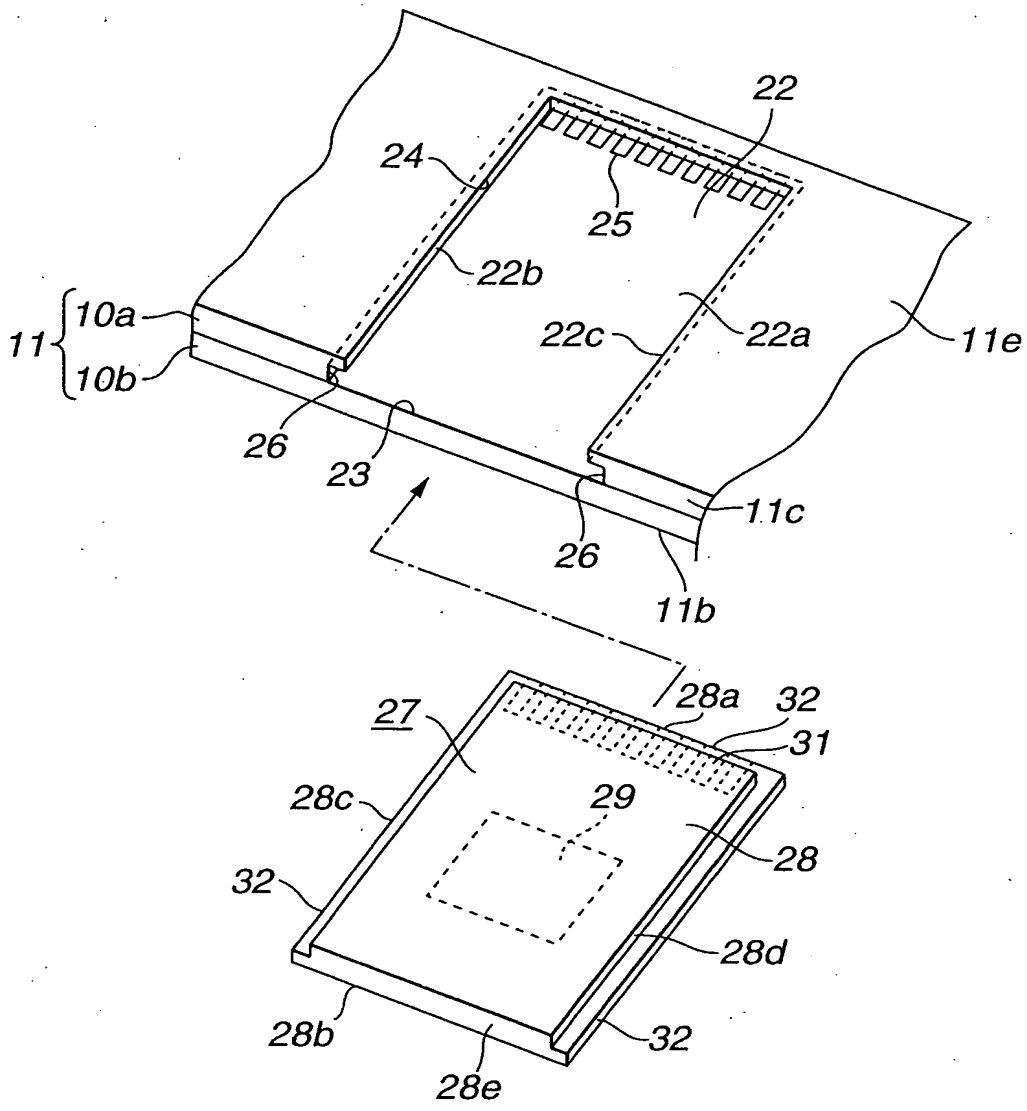
[FIG.6]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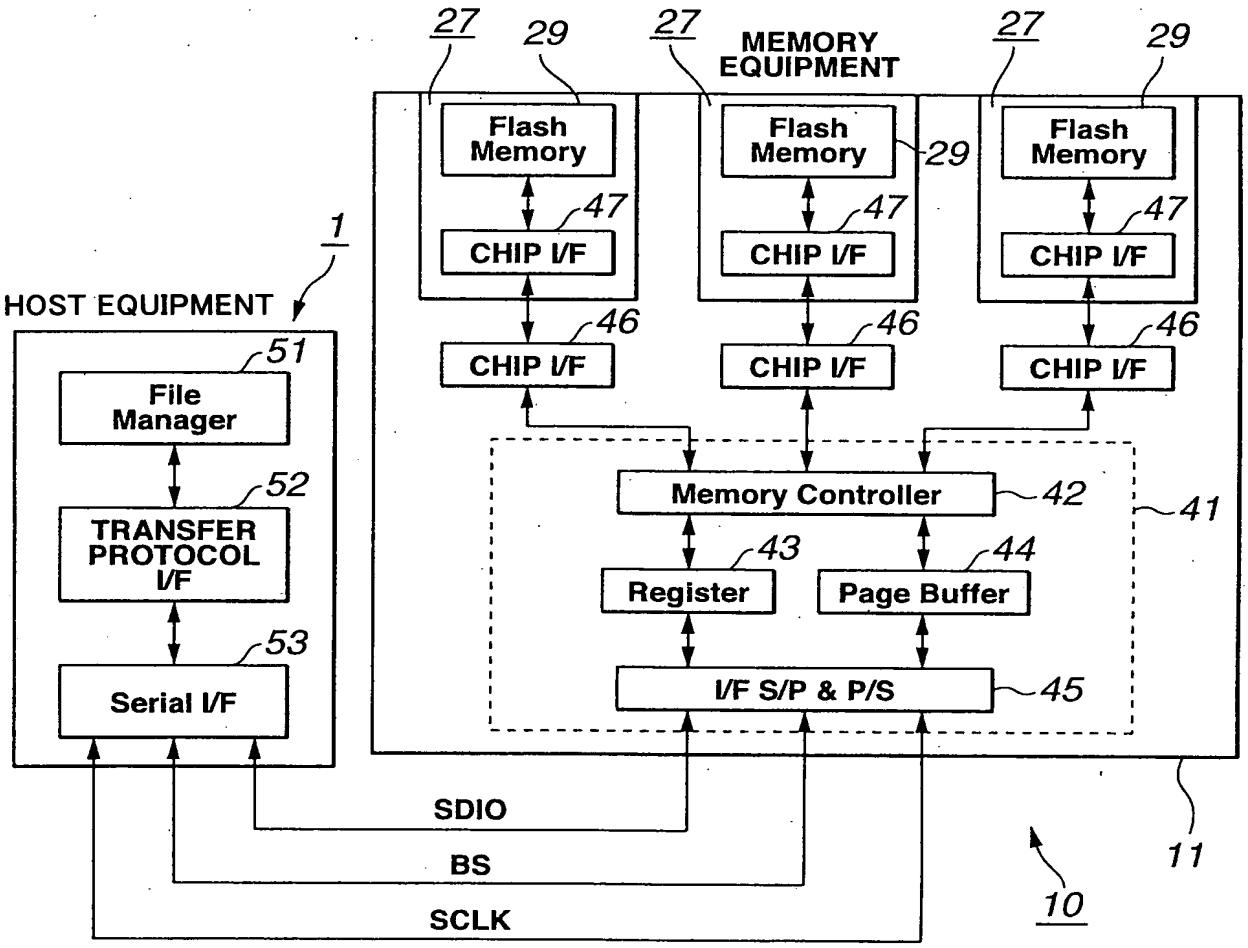
[FIG.7]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MEMORY EQUIPMENT
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Flash Memory
Flash Memory
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Flash Memory
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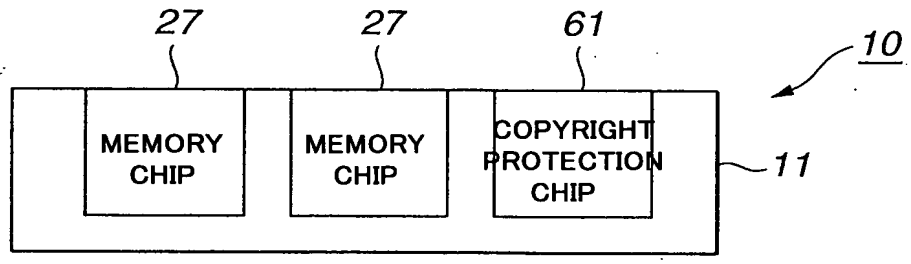
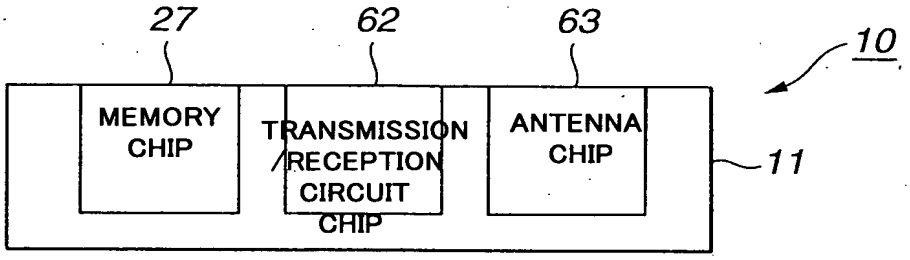
CHIP I/F
CHIP I/F
CHIP I/F
1
46
46
46
CHIP I/F
CHIP I/F
CHIP I/F
HOST EQUIPMENT
51
File Manager
Memory Controller
42
41
52
TRANSFER PROTOCOL I/F
43
44
Register
Page Buffer
53
Serial I/F
I/F S/P & P/S
45
SDIO
BS
SCLK
11
10

[FIG.8]


27
27
61
10
MEMORY CHIP
MEMORY CHIP
COPYRIGHT PROTECTION CHIP
11

[FIG.9]


27
62
63
10
MEMORY CHIP
TRANSMISSION /RECEPTION CIRCUIT CHIP
ANTENNA CHIP
11

[Name of Document] ABSTRACT

[Summary]

[Task]

A memory device having a variable storage capacity depending on the use object by a user to improve convenience in use of the device.

[Means for Solution]

The memory device includes a substantially rectangular casing 11 loaded on a host apparatus 1, memory chips 27 each including a flash memory 29 therein, a terminal unit 13 provided to one side of said casing 11 for electrical connection to said host apparatus 1, loading sections 22 being adapted for loading said memory chips 27 therein, with the number of said loading sections 22 corresponding to the number of the memory chips 27 that may be loaded on said casing 11, and connection terminals 25 provided to said loading sections 22 and configured for being electrically connected to terminals 31 provided to said memory chips 27. The casing 11 includes a semiconductor unit 12 configuring a controller for controlling write and readout of information signals to or from the memory chips 27 loaded in said loading sections 22.

[Selected Drawing] FIG. 2